



***IN THE UNITED STATES PATENT AND TRADEMARK OFFICE***

Applicant: Keiichiro KATA et al.  
Title: PROCESS FOR MANUFACTURING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR WAFER  
Appl. No.: 10/645,782  
Filing Date: 08/22/2003  
Examiner: Unassigned  
Art Unit: 2822

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**  
**UNDER 37 CFR §1.56**

Commissioner for Patents  
PO Box 1450  
Alexandria, Virginia 22313-1450

Sir:

This paper supplements the Information Disclosure Statement submitted on November 13, 2003 enclosing Form PTO/SB/08 listing 10 foreign language documents known to Applicants in order to comply with Applicants' duty of disclosure pursuant to 37 CFR §1.56 together with a copy of each listed document to comply with the provisions of 37 CFR §1.97 and §1.98.

**TIMING OF THE DISCLOSURE**

This supplemental Information Disclosure Statement is being submitted in compliance with 37 CFR §1.97(b), before mailing of the first office action.

### RELEVANCE OF EACH DOCUMENT

The Information Disclosure Statement submitted on November 13, 2003 incorrectly indicated that the relevance of the foreign-language documents was described in the present specification. The relevance of each reference is set forth below.

Reference A1, Japanese laid open utility model application 64-57643 (published on April 10, 1989) was cited by an opponent against the counterpart Japanese patent. This reference discloses a semiconductor chip 10 (Fig. 1a) to be installed on a circuit board 40 (Fig. 1b). The chip 10 includes connection pads 13 located at the periphery of the chip and connection bumps 20 (Fig. 1a and Fig. 3) at the internal area of the chip.

Reference A2, Japanese laid open patent application 4-373131 (published on December 25, 1992), was cited by Japan Patent Office on April 22, 1997 in the examination of the counterpart application of the '304 patent. This reference discloses an assembly of IC chips where external connection lands 2 (in Fig. 1) are arranged in a matrix on the entire surface of each of chip sections on the wafer 3 (in Fig. 2) before scribing the wafer to divide it into the separate chips 1. This is an implementation of prior art chips where the external connection lands 12 (in Fig. 4) were placed only on the edge of the chips 11 (Fig. 4). In either case, the external connection bumps 4 (Fig. 3) or 14 (Fig. 5) are put on the lands. This reference suggests that appropriate circuit elements are previously formed on the surface of the chips 1 and that those elements are then connected to such external connection lands 2 via electrically conductive films.

Reference A3, Japanese laid open patent application 5-267302 (published on October 15, 1993), was cited by the Japan Patent Office on April 22, 1997 in the examination of the counterpart application of the '304 patent. This reference discloses a separate IC chip 1 (in Figs. 1 and 3), which has bumps 3, 13 or 14 in a matrix arrangement. This IC chip is comprised of a plurality of large I/O cells 6 (Fig. 2) arranged in a periphery of the chip and small I/O cells 4 (Fig. 2) in the internal area of the chip. The large I/O cells are connected to bumps in a periphery of the matrix such as bumps 3, 13, or 14. The small I/O cells are connected to bumps 13, 14 or other bumps further inside the matrix of bumps.

Reference A4, Japanese laid open patent application 63-293965 (published on November 30, 1988), discloses a semiconductor chip 4 (Fig. 1) having bumps 5 (Fig. 5).

Reference A5, Japanese laid open patent application 1-173733 (published on July 10, 1989) was cited by an opponent against the counterpart Japanese patent. This reference discloses a wafer 24 (Fig. 1) and chips 43 (Fig. 3), including external electrodes of the chips. The electrodes 40 are formed simultaneously by electro plating with a current path 41 at the scribe lines 42.

Reference A6, Japanese laid open patent application 5-166812 (published on July 2, 1993), was cited by Japan Patent Office on April 22, 1997 in the examination of the counterpart application of the '304 patent. This reference shows a separate IC chip 11 (in Fig. 1). The chip 11 has pads 12 on the periphery of the chip 11, multilayer metal wiring 13, and bumps 14. Some of the bumps are arranged in a center of the chip 11 (Fig. 1).

Reference A7, Japanese laid open patent application 6-112211 (published on April 22, 1994), was cited by Japan Patent Office on November 12, 1997 in the examination of the counterpart application of the '304 patent. This reference discloses an assembly of wafer 1 including chips 2, which are later divided by scribe lines 13 (Figs. 20). The chip 2 has electrodes 4 and bumps 9 on the electrodes 4 via multilayer barrier metal 6, where both electrodes and bumps are on the periphery of the chip (Figs. 9 and 17). Each bump has a portion (9a) on the chip and another portion (9b) beyond the chip for alignment purpose.

Reference A8, Japanese laid open patent application 1-196856 (published on August 8, 1989), discloses a semiconductor wafer 1 (Figs. 1, 7 or 11), on which dicing lines ID (Fig. 7) and chips are provided. The chip has electrodes 2 (Figs. 1, 11) on its surfaces, which electrodes are defined by the patterns 18 (Fig. 7) of a photo mask 15 (Fig. 7). The electrodes 2 are connected via wiring 6 to bumps at the openings 11 (Fig. 11) provided at appropriate bump formation areas on the chip.

Reference A9, Japanese laid open patent application 5-218042 (published on August 27, 1993), was cited by an opponent against the counterpart Japanese patent of the '304 patent. The reference discloses a semiconductor chip 9 (Figs. 1 and 2) including first pads 8 at the periphery, insulation layer 10 over the pads 8, and second pads 11 above the insulation layer and located at the internal area of the chip.

Reference A10, Japanese laid open patent application 63-86458 (published on April 16, 1988) was cited by Japan Patent Office on November 12, 1997 in the examination of the counterpart application of the '304 patent. The reference discloses an assembly of wafer 1 later divided into chips 17 or 19 (Figs. 4 or 5). Each chip 17 or 19 has pads 7 at the periphery and bumps 15 on the pads.

An English translation of the foreign-language documents is not readily available. However, the absence of such translation does not relieve the PTO from its duty to consider the submitted foreign language documents (37 CFR §1.98 and MPEP §609).

Applicants respectfully request that any listed documents be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 provided with the Information Disclosure Statement of November 13, 2003, be returned in accordance with MPEP §609.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 CFR §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

Respectfully submitted,

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